

Notice of References Cited	Application/Control No. 10/748,285	Applicant(s)/Patent Under Reexamination JOURDAN, STEPHAN J.	
	Examiner George D. Zalepa	Art Unit 2183	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,304,962	10-2001	Nair, Ravindra K.	712/240
	B	US-			
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	D	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Eric Rotenberg, Steve Bennett, James E Smith, "Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching", 1996, IEEE, Pg. 1, 5-6
	V	Sanjay Jeram Patel, "Trace Cache Design for Wide-Issue Superscalar Processors", 1999, University of Michigan, Pg. 74-76
*	W	Andrew S. Tanenbaum. Structured Computer Organization, 1984. Pg. 10-11
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.